REMARKS/ARGUMENTS

Reconsideration and allowance are respectfully requested. No new matter is added by this amendment. Because a Request for Continued Examination is being filed herewith, it is believed that finality is now withdrawn and that the amendments can properly be entered.

Rejection Under 35 U.S.C. § 112, Second Paragraph

It is alleged that the preamble of claim 1 recites data compaction but the body of claim 1 does not include a step that performs data compaction. It is believed that the amendments to claim 1 should overcome the Examiner's concerns.

Art-Based Claim Rejections

Claims 1-17, 19, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 09/920,930 to Kurooka, et al. ("Kurooka"), in view of U.S. Patent Application No. 6,816,989 to Timothe Litt ("Litt"), and further in view of U.S. Patent No. 5,355,487 to Keller, et al. ("Keller"). Claims 20-22, 24-26, and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Litt in view of Keller. Claims 18 and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurooka in view of Litt, further in view of Keller, and still further in view of U.S. Patent No. 6,754,599 to Swoboda, et al. ("Swoboda"). Claims 29-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Litt in view of Swoboda.

It is noted that the Kurooka application is not itself prior art. It is understood that the Examiner actually intends to refer to the publication of that application, which is publication no. 2002/0162055 A1, or to the issued patent from that application, which is U.S. Patent No. 6,813,732. Accordingly, all further references to Kurooka herein mean publication no. 2002/0162055 A1.

Applicants respectfully traverse the rejections in view of the amendments herein and the following remarks.

Independent Claim 1

Independent claim 1 as amended recites selecting data of interest from a first sample, wherein the data of interest is a subset of bits of the first sample and includes at least first and second portions separated from each other by at least one bit that is not part of the data of interest; and

storing the data of interest from the first sample in said first buffer if it is determined that residual storage space in the first buffer exists, such that the first and second portions of the data of interest as stored is no longer separated from each other by the at least one bit.

It is submitted that none of Kurooka, Litt, or Keller, either alone or in combination as proposed, teaches or suggests this amended claim feature.

The Office Action refers to Kurooka at paragraph [0028], which discusses bit width conversion. However, this bit width conversion does not store data in the manner now claimed. It is noted that the bit width conversion of Kurooka merely converts 8-bit parallel outputs to 4-bit parallel outputs. This does not allow for storing portions of data separated by another bit to be stored together without the separation, as claimed.

Nor would the proposed modification of Kurooka by Litt and Keller make up for this deficiency.

For at least this reason, it is submitted that claim 1 is allowable over Kurooka, Litt, and Keller, either alone or in combination as proposed.

Independent Claim 20

It is submitted that claim 20 is also allowable for at least similar reasons as discussed above with regard to claim 1.

Independent Claim 29

Independent claim 29 recites two steps: (1) determining a trace data fill rate of each of a plurality of trace data chains; and (2) determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates.

The Office Action asserts Litt as teaching step (1). Litt discloses a circuit in which data from multiple sources 70, 80, 90 is multiplexed into a plurality of parallel smart buffers 225. The smart buffers 225 decide what data to keep based on the importance of each data packet and how full that data packet is. Litt, col. 3, lines 49-56. Arbitration logic 250 then selects data from the various smart buffers 225 based on the importance of the data, the "pressure" that each smart buffer is under, and the workload of an output driver 135. Litt, col. 6, lines 15-18 and 35-42; col. 12, lines 29-34.

As Applicants and the Examiner appear to agree, Litt does not teach or suggest pin scheduling. Rather, the arbitration logic 250 of Litt sends data to an output driver 135 without regard to pin assignment.

The Office Action proposes to modify arbitration logic 250 of Litt to take into account pin assignment by adding a pin management function as disclosed in Swoboda. The Office Action proposes to further modify arbitration logic 250 to take into account the data fill rates of trace chains (i.e., sources 70, 80, 90).

The basis for the Office Action's motivation to combine lies in the assertion that:

> "Litt teaches arbitration logic selecting between plural trace chains (each smart buffer addressing one trace chain) ... based on fill rates (where the higher fill rate will fill smart buffer faster causing a distress signal to be serviced by arbitration logic first)...."

Office Action, p. 4. Respectfully, however, Litt does not teach this at all. In Litt, there is not a smart buffer for each trace chain. Instead, a front-end multiplexer 215 interfaces between the plurality of sources and the smart buffers, sending data to various smart buffers as appropriate. While it is true that arbitration logic 250 can detect whether a smart buffer is "under pressure," this pressure is not related to the data fill rate of any particular source. Again, that is because a given smart buffer is not associated with a given source. Rather, the smart buffers are a shared resource because of the intervening front-end multiplexer 215.

Thus, in Litt, arbitration logic 250 is completely isolated from knowing about the data fill rates of given sources. There is simply no teaching of selecting smart buffers based on any property at all of the sources; arbitration logic 250 is aware only of the smart buffers themselves. Respectfully, the proposed modification has no basis in Litt. Nor does the proposed modification have a basis in Swoboda. Swoboda mentions dynamic pin assignment but says little more about the subject, and certainly does not discuss how such dynamic pin assignment would operate.

Even if the lack of motivation were put aside, the proposed combination would still be missing a cause-and-effect link between trace chain data fill rates and a pin assignment schedule, as required by claim 29. At best, arbitration logic 250 as proposed to be modified might select pins based on smart buffer pressure. However, smart buffer pressure is unrelated to data fill rates of each of a plurality of trace chains, as claimed.

Independent Claims 30 and 31

It is submitted that claims 31 are also allowable for at least similar reasons as discussed above with regard to claim 29.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

It is respectfully submitted that this application is in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better form for allowance, the Examiner is respectfully urged to telephone Applicants' undersigned representative at the below-listed number.

Respectfully submitted,

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